ABSTRACT OF THE DISCLOSURE

A semiconductor memory includes: a p-type semiconductor (p-type semiconductor film on a substrate, a p-type well region in a semiconductor substrate, or an insulator); a gate insulating film formed on the p-type semiconductor; a gate electrode formed on the gate insulating film; two charge storage sections formed on side walls of the gate electrode; a channel region provided below the gate electrode; and a first n-type diffusion layer region and a second n-type diffusion layer region provided to sides of the channel region, wherein: the charge storage sections are arranged to change an electric current flow between the first n-type diffusion layer region and the second n-type diffusion layer region under application of a voltage to the gate electrode according to the quantity of electric charges stored in the charge storage sections; and the first n-type diffusion layer region is set to a reference voltage, the other n-type diffusion layer region is set to a voltage greater than the reference voltage, and the gate electrode is set to a voltage greater than the reference voltage. Thus, the semiconductor memory obtained is capable of 2 bit operation and easy to miniaturize.